

Ecole polytechnique fédérale de Lausanne EPFL School of Computer and Communication Science (IC)

Programming Non-Volatile Memory

James Larus Professor and Dean, IC October 23, 2018

James Larus

Joint Work



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David Aksun, PhD student

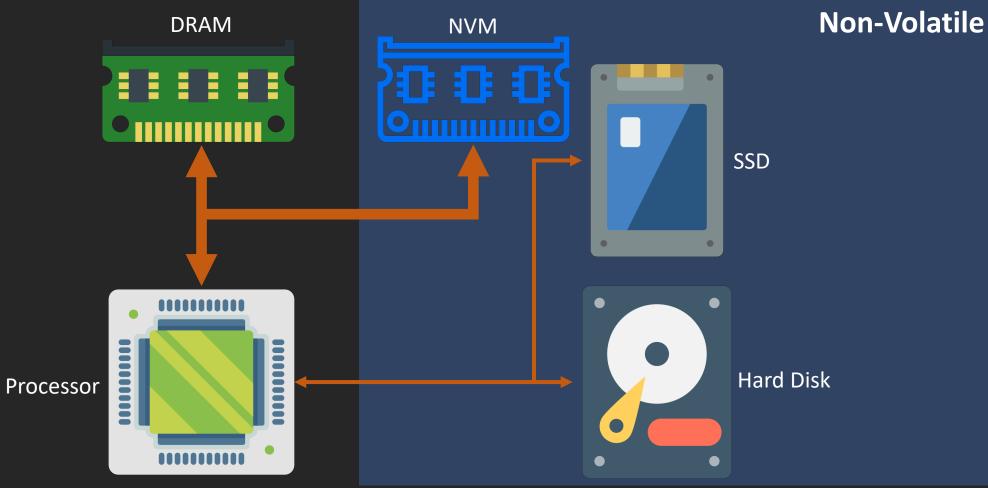




Background on NVM



Non-Volatile Memory (NVM)





NVM Characteristics







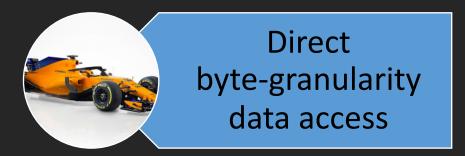




Only consumes power during memory access

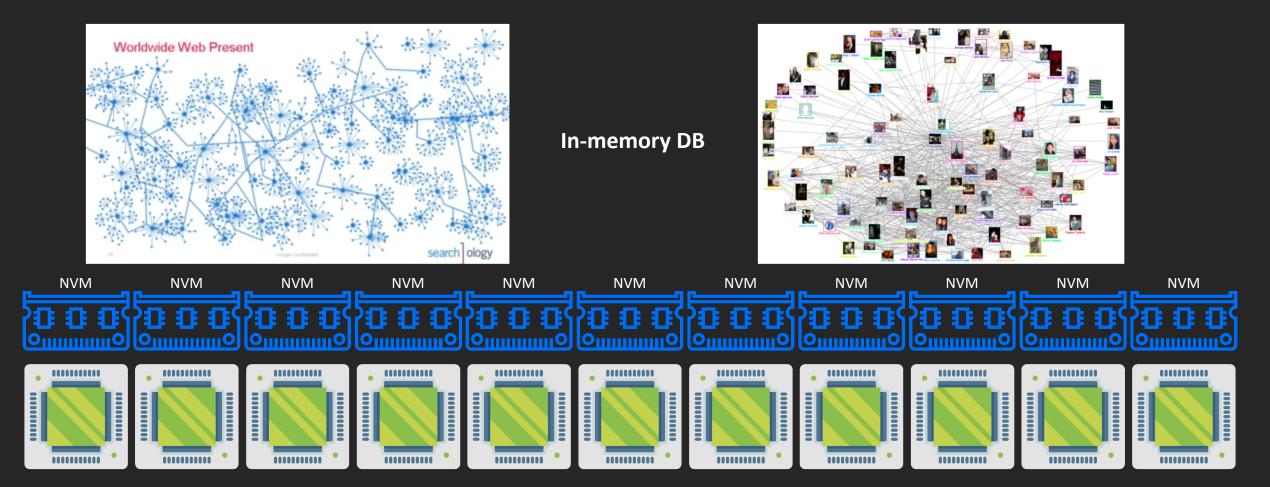


Retains data without power





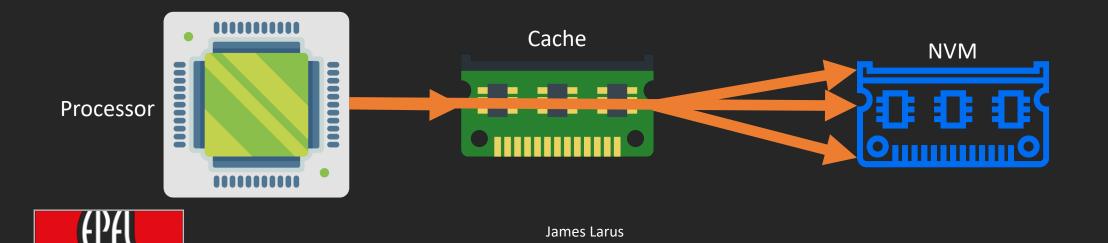
NVM Use Case



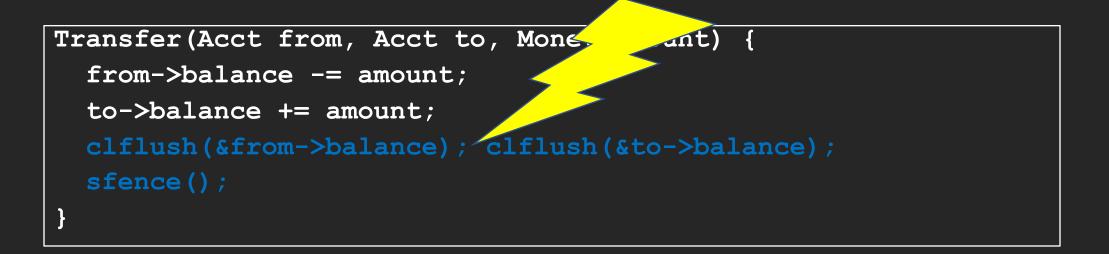


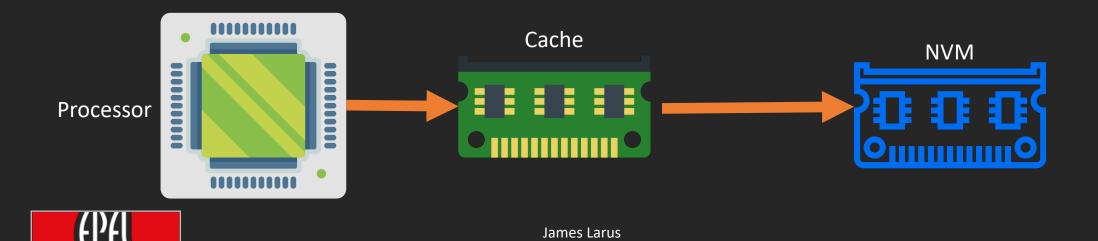
How Not to Program NVM

```
Transfer(Acct from, Acct to, Money amount) {
  from->balance -= amount;
  to->balance += amount;
}
```



Programming NVM, version 1

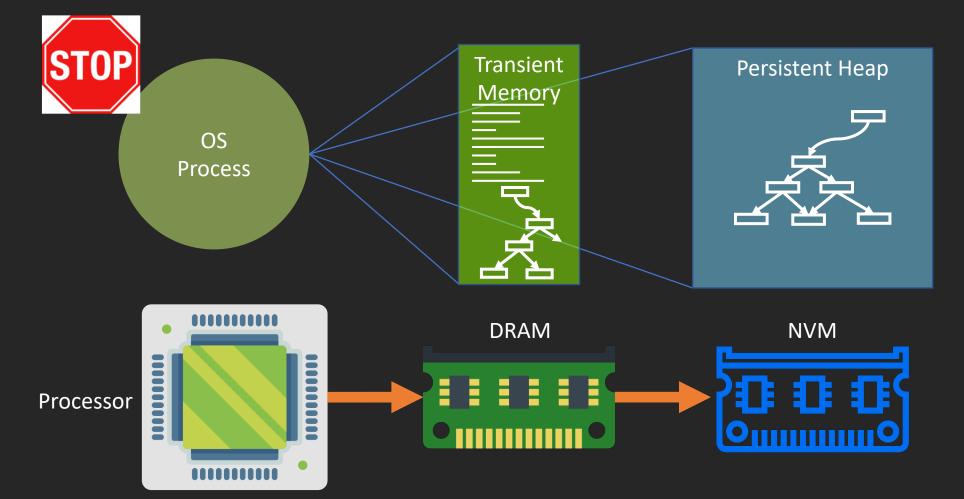




Programming NVM, version 2

```
Transfer (Acct from, Acct to, Money amount) {
   atomic {
     from->balance -= amount;
     to->balance += amount;
     clflush(&from->balance); clflush(&to->balance);
     sfence();
 }
         Cache
                                                    NVM
      Processor
```

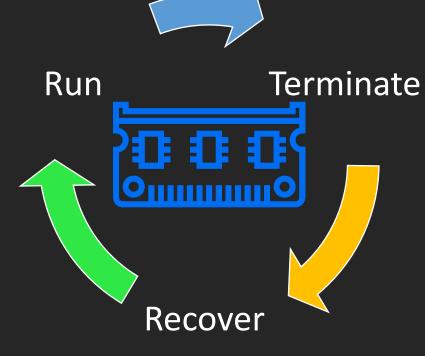
NVM Usage





NVM Lifecycle

1. Processes accesses NVM with individual load and store instructions



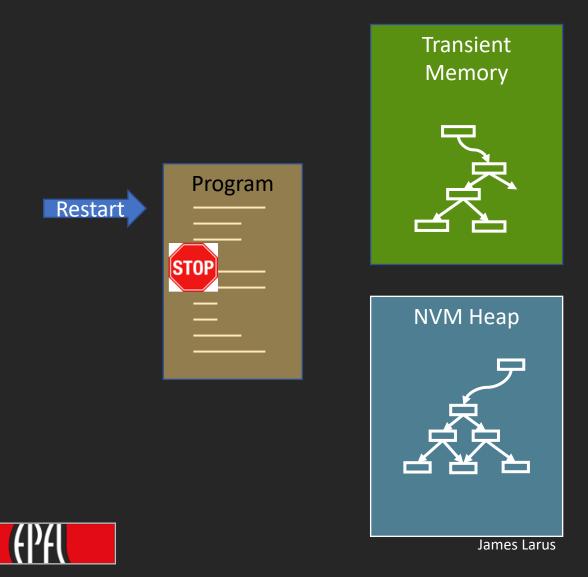
3. Need to ensure that NVM state is consistent in the environment in which execution restarts.

2. NVM must record a consistent memory state <u>before</u> termination, whether planned or unexpected



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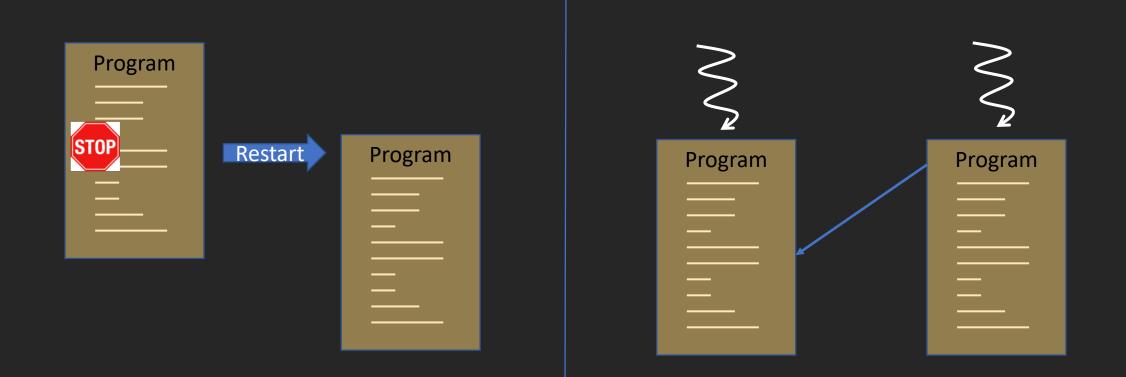
When is NVM "Consistent"?



- NVM is consistent when restarted program produces same output as some execution of the program without a premature termination
- In general, error recovery is difficult if memory state does not satisfy program invariants
- Programs transition between invariant-satisfying states, but states in between are inconsistent (and impossible to recover)
- NVM should not be left in one of these inconsistent states

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Similar to Concurrency



Key difference: execution stops and only part of state is preserved. Some parallelization optimizations (such as privatization) can cause errors.



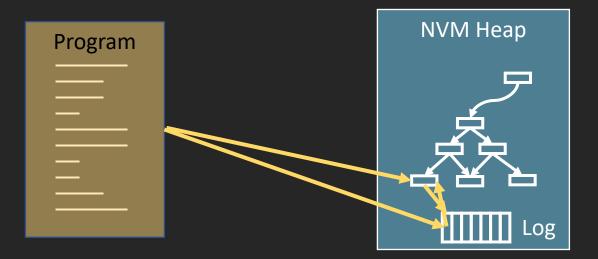
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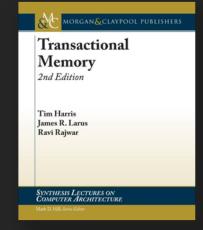
Durable Transactions

```
Transfer(Acct from, Acct to, Money amount) {
   atomic {
    from->balance -= amount;
    to->balance += amount;
   } //clflush(&from->balance); clflush(&to->balance); sfence();
}
```



Software Transactional Memory





Undo log – save contents of overwritten memory locations, so they can be restored if transaction fails

Redo log – save updated values, so they can applied to memory if transaction succeeds



End of background

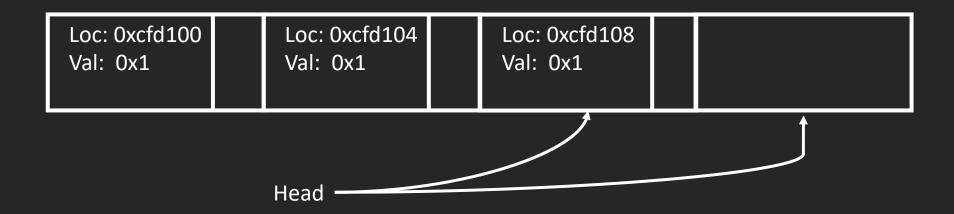


Outline

- Efficient Logging
- Checkpointing with InCLL
- NVM Recovery



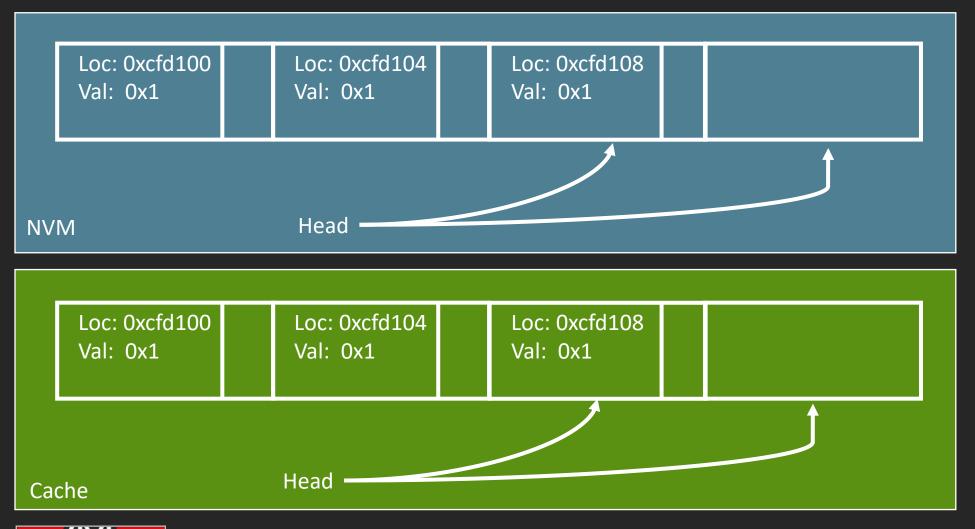
Efficient Logging



Cohen, Friedman, Larus. Efficient Logging in Non-Volatile Memory by Exploiting Coherency Protocols. OOPSLA 2017.

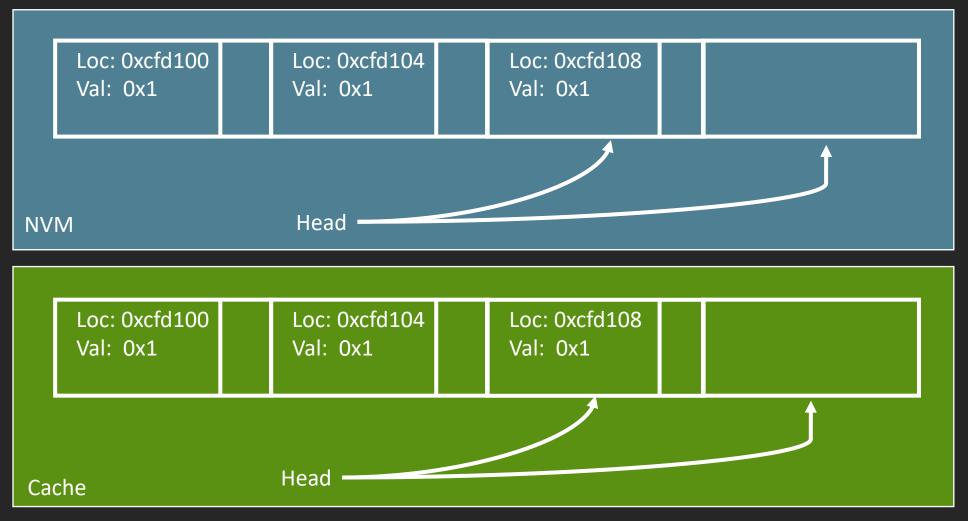


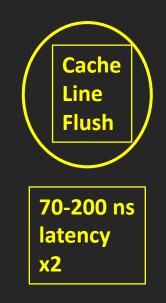
NVM, Caches, and Logging



Unordered Write-Back

NVM, Caches, and Logging

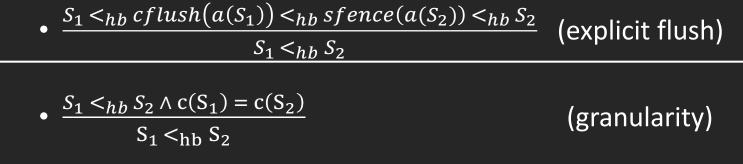




NVM Consistency Model

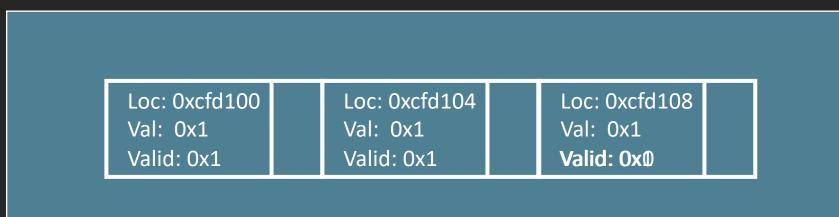
- Assumption 1: If store instruction S₁ becomes visible to other threads before instruction S₂, then the value written by S₁ reaches the cache before the value written by S₂
- Assumption 2: A cache line is transferred from the cache to the NVM atomically

• Persistent ordering





Validity Bit



Loc: 0xcfd100	Loc: 0xcfd104	Loc: 0xcfd108	
Val: 0x1	Val: 0x1	Val: 0x1	
Valid: 0x1	Valid: 0x1	Valid: 0x0	

Assume: log entry fits in cache line (64 bytes) and at least one bit (of 512) is unused

Log entry is valid if bit is set (unset)

Requires only 1 cache flush



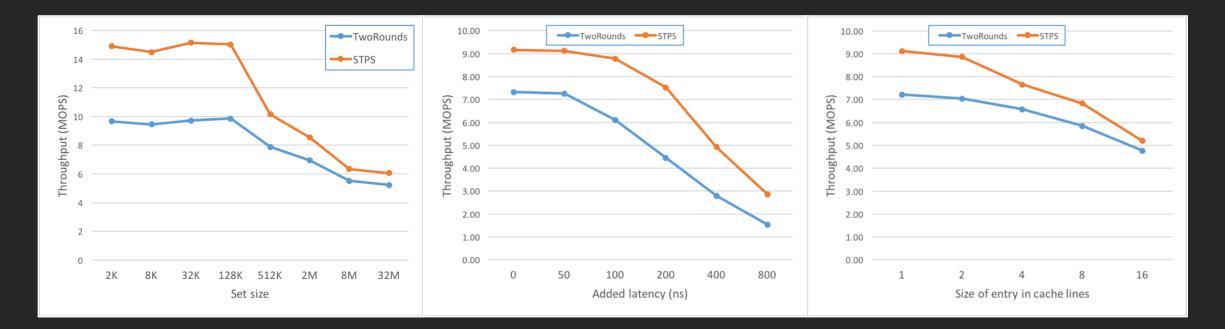


What If Validity Bit Does Not Fit?

- Randomization
 - Initialize log memory with 64-bit random value
 - Write log entry in order
 - If last word is not random value, then entry is valid (with high probability)
- Flexible validity bit
 - Find first bit different between old cache line and new value
 - If bit exists, use it as validity bit (otherwise, doesn't matter)
 - Store bit position in external table
- Almost always can find validity bit
 - x64 address have 15 unused bit at top and typically 2/3 unused bits at bottom
- More details and examples in paper



Performance



Single-Trip Persistent Set (STPS) Two cache flushes (TwoRounds)

YCSB write heavy benchmark (50% writes)



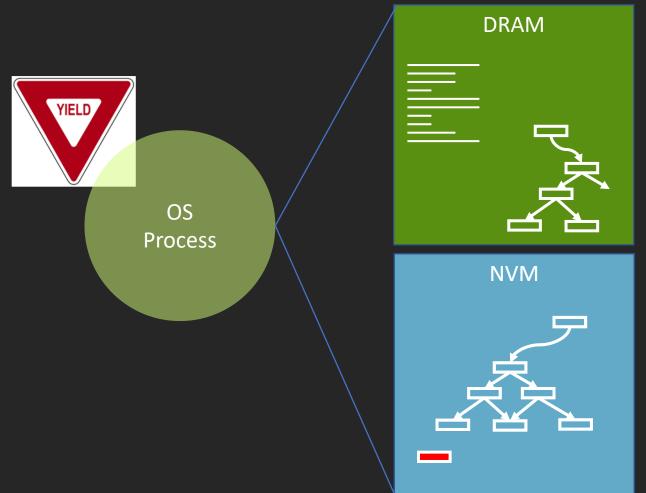
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Checkpointing



Checkpointing used in high-performance computing (HPC)

Problems:

- Long pause while copying heap
- Recovery time proportional to checkpoint interval



Fine-Grain Checkpointing of Masstree

- Masstree is cache-efficient combination of trie and B+ tree
 - Mao, Kohler, Morris. Cache craftiness for fast multicore key-value storage. EuroSys '12, 2012
- Used in Silo in-memory DB, key-value stores, etc.

• Make Masstree persistent by storing data structure in NVM

Cohen, Aksun, Larus. **Fine-Grain Checkpointing with In Cache Line Logging**. Submitted for Publication.



Epochs

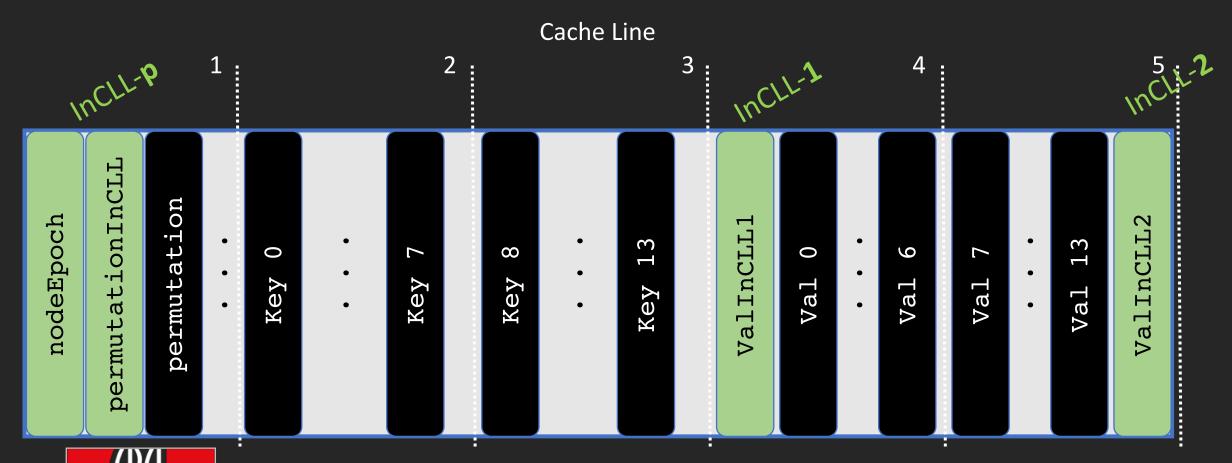
Faisal Nawab, et al., **Dalí: A Periodically Persistent Hash Map, DISC** 2017.

- Checkpoint with 64 ms epoch
 - Masstree uses this interval for allocating/reclaiming nodes
- Execute wbinvd instruction to flush <u>entire</u> cache (to NVM)
 - 430 550µs (< 1%)
- Failure during epoch causes execution to restart after previous epoch
- Need to undo changes written during a failed epoch
 - In cache-line log (InCLL)
 - Separate undo log for complicated, infrequent cases



Masstree Leaf Node

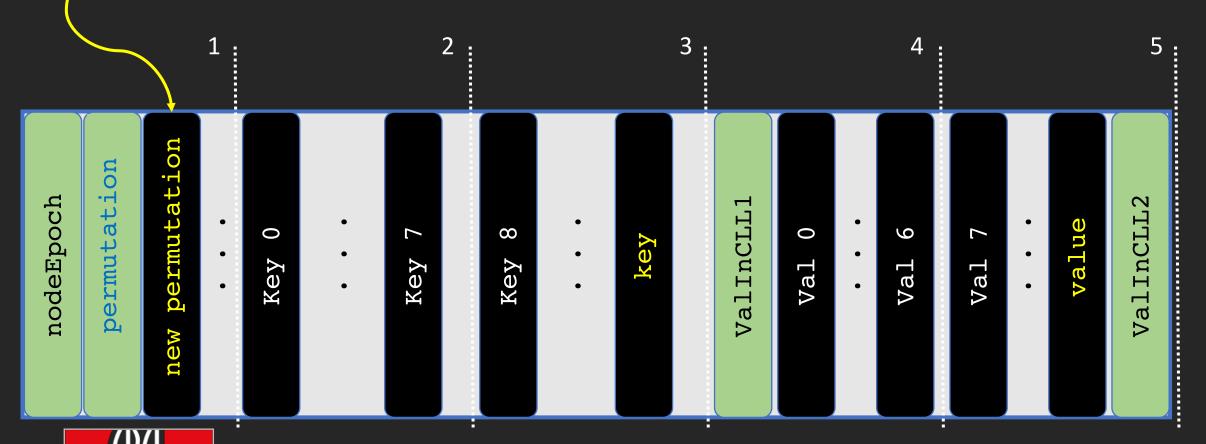
14 keys, values (1 fewer than standard)



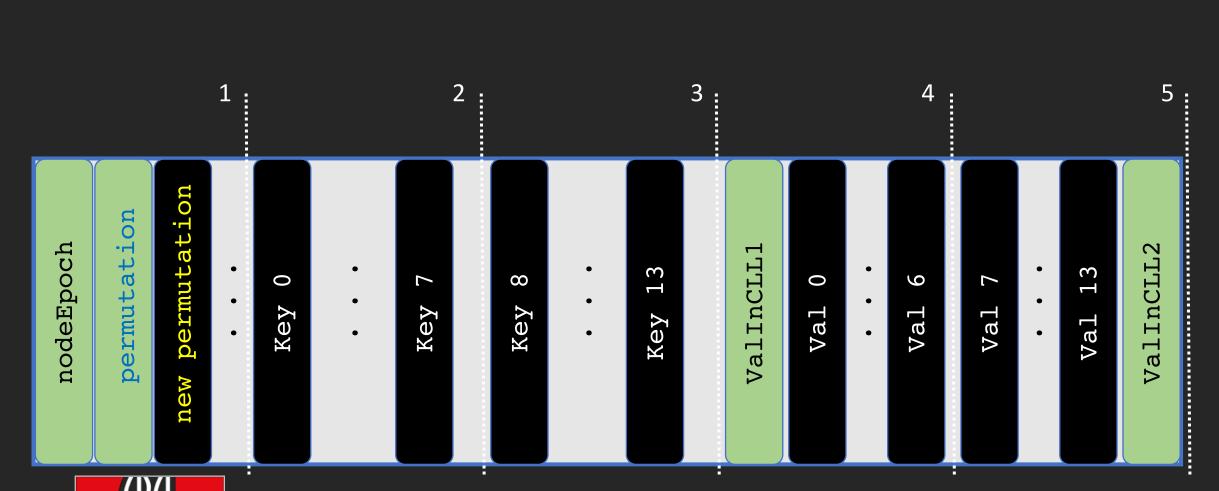
Insert (With Empty Value Slot)

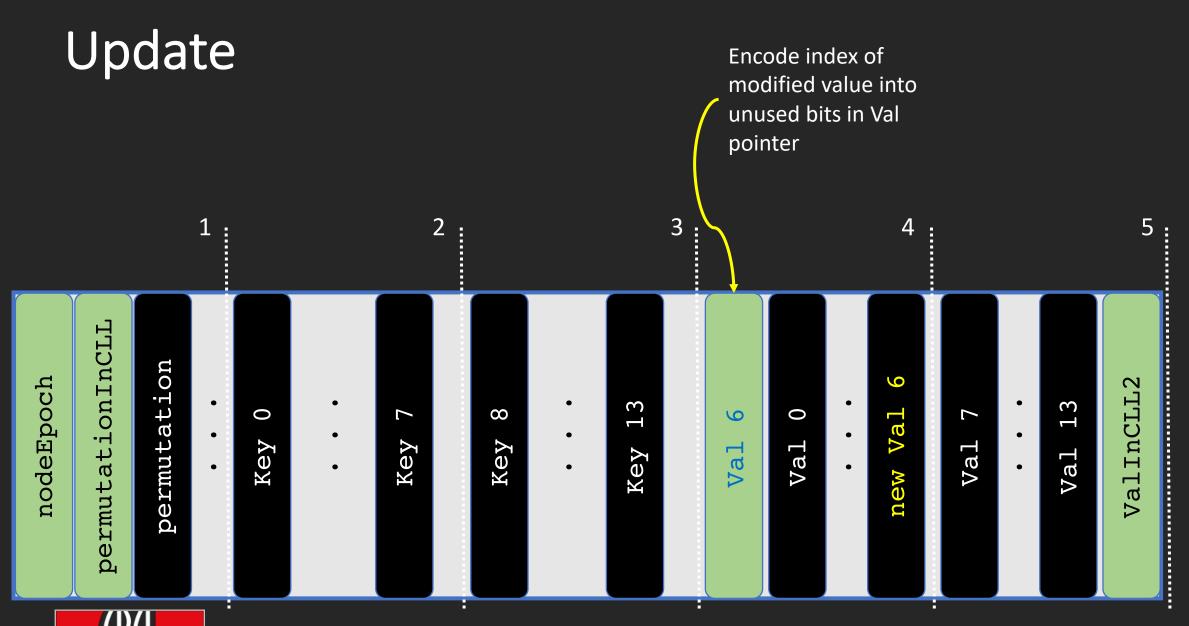
map of empty keys

If no empty slot, then split node Use undo log for node splitting









Sequences of Operations

Mixed sequences of insert delete require redo logging because InCLL can only hold one value

Also encode epoch in unused bits

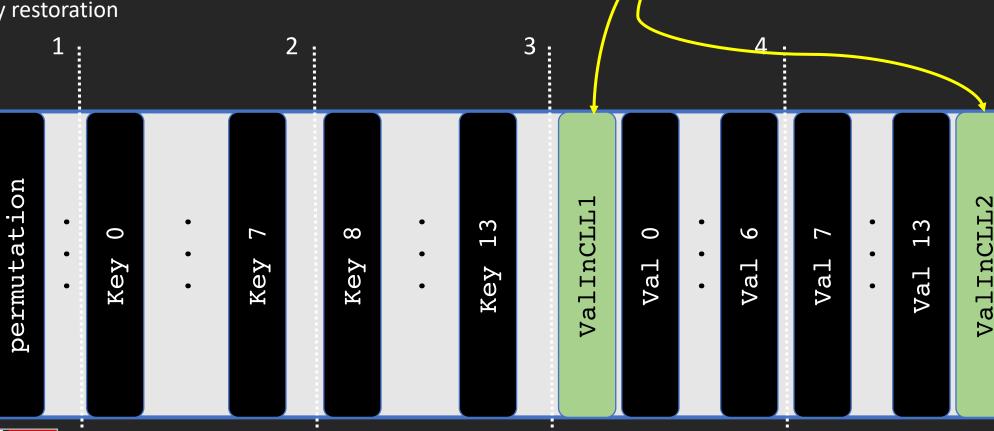
Epoch in which permutation was checkpointed

- Only copy permutation when Epoch differs (once per epoch)
- Allows lazy restoration

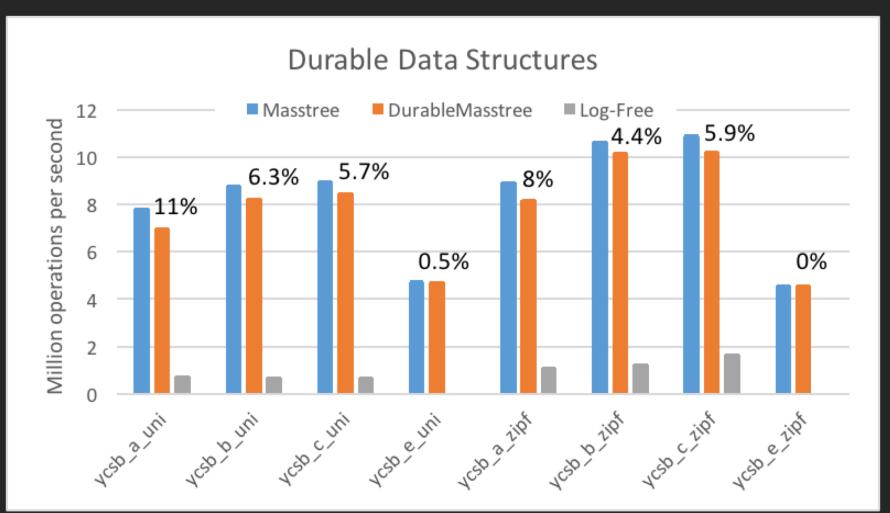
ionInCLL

permutat

nodeEpoch

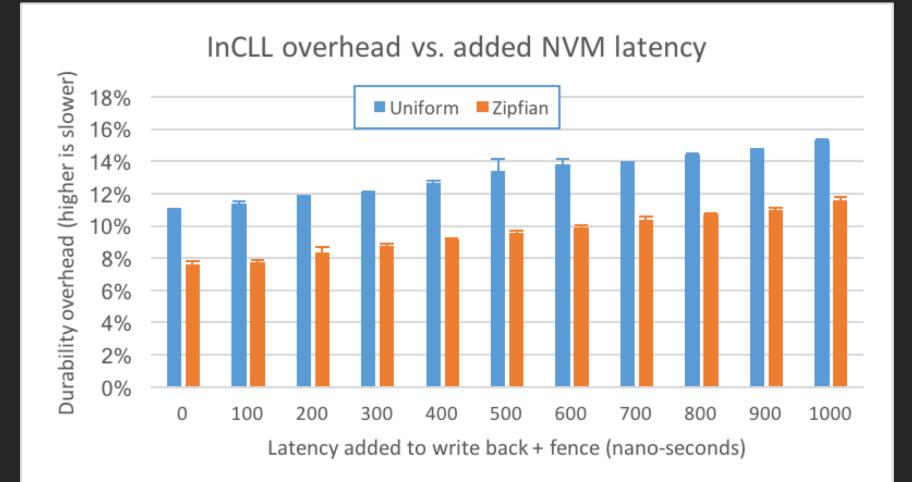


Performance





Performance (Added NVM Latency)

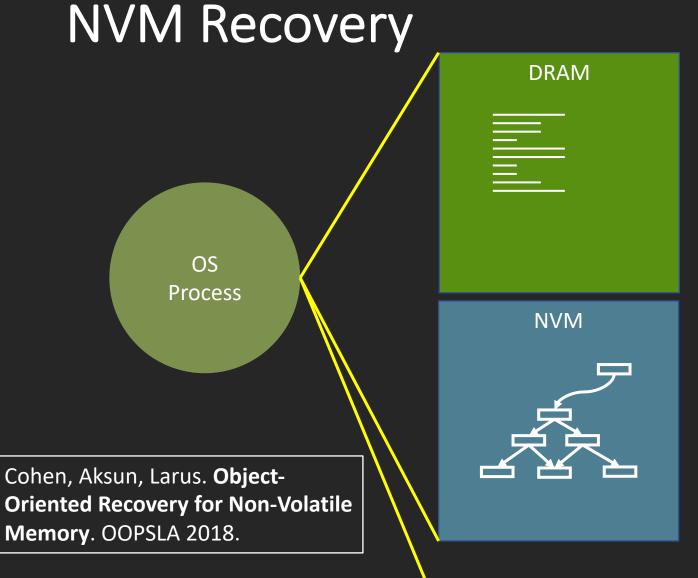




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Persistent objects point to methods

 Code may be loaded at different address because of ASLR, debugger, profiler, code changes, ...

Persistent store may be mapped to different virtual address

Persistent data must be consistent in recovered process, as well as being consistent when original process fails



Potential Inconsistencies

- Transient objects pointed to from NVM
 - TCP sockets, locks, thread IDs, ...
- Pointers between persistent objects if NVM mapped to different location
- Pointers to code and read-only data if text segment mapped differently



Previous Solutions

- Ignore the problem
 - If NVM maps to different location, quit...
 - Oops, there goes your data!
 - If text maps differently, continue...
 - Oops, there goes your data!
 - If you use an old lock, fail...
 - Oops, there goes your data!
- Use offsets between persistent objects instead of addresses
 - Memory access becomes more expensive
 - Requires extensive code changes

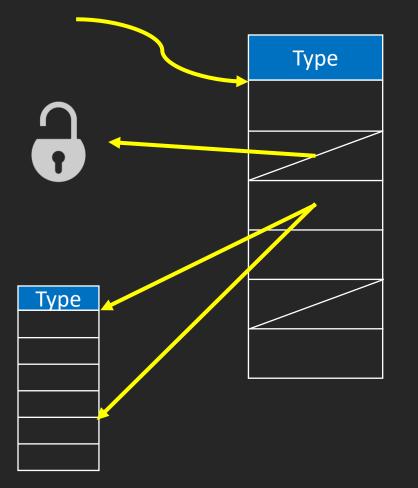


NVMReconstruction C++ Extension

```
struct kp_vt_struct {
 kp_kvstore *parent; // back-pointer to parent kvstore
  transient pthread mutex t *lock; // lock for this version table
   • • •
 reconstructor(kp vt struct* o) {
    assert(kp_mutex_create("(*new_vt)->lock", &(o->lock)) == 0);
void main() {
 kp vt struct *new vt = pnew kp vt struct;
 • • •
 pdelete new vt;
```



Reconstructing an Object

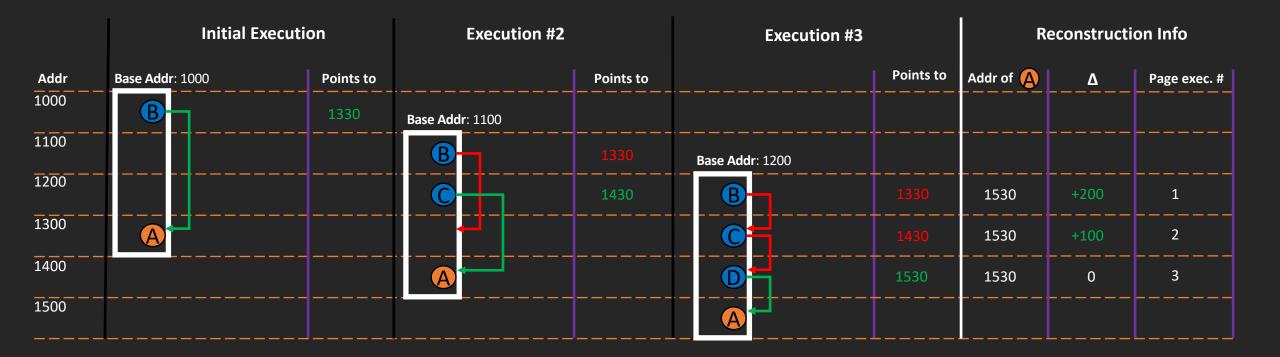


- Every persistent object has a type header
 - LLVM extension
- Zero transient fields
- Relocate pointers
 - Inter NVM
 - To code and read-only data
- Run reconstructor function

Similar to relocation in garbage collector, except...

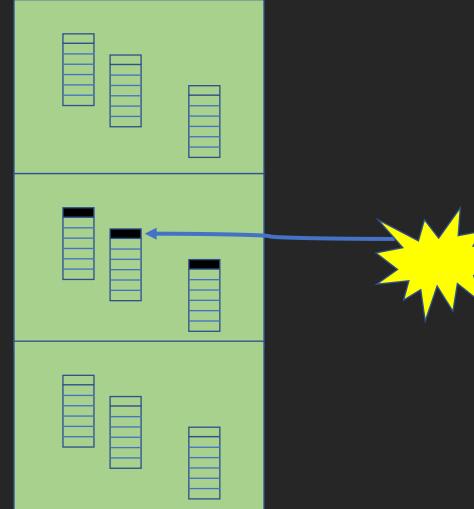


Failure During Relocation





Startup Latency

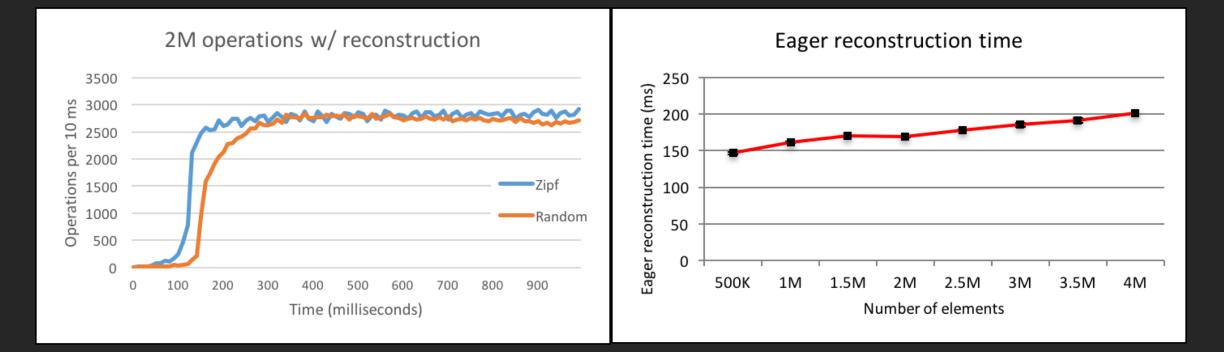


Lazy Reconstruction

- Use VM page protection to detect first access to object
- Reconstruct all objects on page



Performance Overhead



Key-value store implemented in Atlas. 1GB NVM heap. YCSB write-heavy workload (50% writes).



Conclusion

- NVM is persistent, directly accessible main memory
 - Well suited for very large in-memory data structures (DB, graphs, etc.)
- Programs must be aware of "NVMness" to allow recovery
- Caches in existing memory systems make consistency expensive
 - Key insight: memory consistently transfers entire cache line to NVM
- How much can we pack into a cache line?
 - More than you think
- But, don't forget recovery!

